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ABSTRACT

The interface properties and energy band alignment of SiO_2/GaN metal-oxide-semiconductor (MOS) structures fabricated on N-polar GaN(000$\bar{1}$) substrates were investigated by electrical measurements and synchrotron-radiation x-ray photoelectron spectroscopy. They were then compared with those of SiO_2/GaN MOS structures on Ga-polar GaN(0001). Although the SiO_2/GaN(000$\bar{1}$) structure was found to be more thermally unstable than that on the GaN(0001) substrate, excellent electrical properties were obtained for the SiO_2/GaN(000$\bar{1}$) structure by optimizing conditions for post-deposition annealing. However, the conduction band offset for SiO_2/GaN(000$\bar{1}$) was smaller than that for SiO_2/GaN(0001), leading to increased gate leakage current. Therefore, caution is needed when using N-polar GaN(000$\bar{1}$) substrates for MOS device fabrication.

Gallium nitride (GaN) is a direct wide-bandgap semiconductor that is widely used as a light-emitting material for highly efficient blue light-emitting diodes and blue-violet laser diodes. GaN and related materials are also expected to be used as semiconductor materials for next-generation power electronic devices because of their excellent electrical properties such as high breakdown electric field and high electron saturation velocity.[1–3] In particular, high electron mobility transistors (HEMTs), which use two-dimensional electron gas generated at an AlGaN/GaN heterointerface, are commercialized as power amplifiers for high frequency applications.[4–6] Furthermore, since conventional AlGaN/GaN HEMTs have suffered from large gate leakage current through the Schottky-gate structures, metal-oxide-semiconductor (MOS)-gate GaN HEMTs have been studied as an alternative.[7–9] In addition to AlGaN/GaN HEMTs, vertical GaN MOS field-effect transistors (MOSFETs) such as double-diffused MOSFETs (DMOSFETs) and trench-type MOSFETs have also been investigated.[10–14] For next-generation GaN MOS power devices as described above, it is essential to form high-quality MOS structures with low defect density and long-term reliability.

The wurtzite GaN lacks inversion symmetry; hence, spontaneous polarization occurs along the *c*-axis direction. The polarization of the Ga-polar GaN(0001) surface is opposite to that of the N-polar GaN(000$\bar{1}$) surface. Most prior research on GaN devices focused on materials and heterostructures fabricated on the GaN(0001) surface. The application of the GaN(000$\bar{1}$) surface has also attracted attention in subsequent years. One of the reasons for this is that N-polar GaN HEMTs, whose structure consists of GaN/AlGaN/GaN(000$\bar{1}$), can operate at a higher frequency than Ga-polar devices.[15] For high frequency operation, this structure offers advantages such as a strong back-barrier, low-resistivity Ohmic contact, and improved scalability.[16] By utilizing these advantages, N-polar GaN HEMTs with operating frequencies above 90 GHz have been demonstrated.[17,18] An additional advantage of the GaN(000$\bar{1}$) surface is its high thermal stability.[19] This property is beneficial in p-type ion implantation into GaN in which Mg ions are used as p-type dopants. After Mg ion implantation, the GaN substrate needs to be annealed at high temperatures exceeding 1000 °C to activate implanted Mg atoms as acceptors.[20] At such high temperatures, the GaN surface is damaged by nitrogen desorption from the surface.[21] It has been previously reported that when Mg ions are implanted into the GaN substrate and annealed at high temperatures, the GaN(0001) surface deteriorates severely, whereas the degradation of the GaN(000$\bar{1}$) surface is

suppressed and the GaN(000$\bar{1}$) substrate exhibits p-type conductivity.[19]

Despite the advantages of fabricating devices on N-polar GaN(000$\bar{1}$) surfaces as discussed above, there are remaining concerns. For applications such as MOS-type power devices, a large conduction band offset at the oxide/GaN interface is desirable for suppressing gate leakage current. This is because the lower the conduction band offset, the larger the leakage current, which flows through the MOS structure at low gate bias. For SiC-based devices, although the field-effect mobility of SiO_2/SiC MOSFETs fabricated on the C-face SiC(000$\bar{1}$) is higher than that on the Si-face SiC(0001),[22] the conduction band offset of the SiO_2/SiC(000$\bar{1}$) structure is smaller than that of the SiO_2/SiC(0001) structure.[23] This indicates that the use of C-face SiC(000$\bar{1}$) substrates degrades the reliability of MOS devices.[24] Thus, a similar problem may occur in the N-polar GaN(000$\bar{1}$). However, there are few reports on the electrical characterization of MOS devices fabricated on N-polar GaN(000$\bar{1}$) substrates.[25–27] In this study, we investigate the electrical properties of SiO_2/GaN MOS structures fabricated on an N-polar GaN(000$\bar{1}$) surface and evaluate the energy band structures by means of synchrotron-radiation x-ray photoelectron spectroscopy (SR-XPS).

A freestanding N-polar GaN(000$\bar{1}$) substrate grown by hydride vapor phase epitaxy (HVPE) was used, with a doping concentration (N_D) of 6×10^{16} cm^{-3}. In addition, an epilayer grown by metalorganic vapor phase epitaxy (MOVPE) on an HVPE-grown freestanding Ga-polar GaN(0001) substrate was prepared for comparison. The N_D of the epilayer was 3×10^{16} cm^{-3}. The process flow of the sample fabrication is shown in Fig. 1. First, the HVPE-grown N-polar GaN substrates were ultrasonicated with acetone and cleaned with hydrofluoric acid (HF). The polishing damage on the HVPE-grown N-polar GaN(000$\bar{1}$) surface was carefully removed by low-damage inductive coupled plasma-reactive ion etching (ICP-RIE) and subsequent plasma oxidation. Specifically, the N-polar GaN surface was etched by about 500 nm under the conditions of ICP power of 50 W and a substrate bias power of 4 W in a BCl_3/Cl_2 gas mixture. Then, a few nm of the GaN surface was removed at a substrate bias power of 1 W.[28] After the gas mixture was evacuated, the etched GaN surface was subsequently oxidized by oxygen plasma at a chamber pressure of 1 Pa, ICP power of 50 W, and a substrate bias power of 1 W. Finally, the oxide layer was removed by wet-etching with an aqua regia and HF. After surface preparation, the SiO_2 films (50–65 nm) were deposited as a gate insulator by plasma-enhanced chemical vapor deposition (PECVD) in a gas mixture of tetraethyl orthosilicate (TEOS) and O_2 at a substrate temperature of 370 °C.[29] Next, post-deposition annealing (PDA) was carried out at temperatures ranging from 200 to 800 °C for 3 min in a nitrogen atmosphere. Ni gate electrodes and Al back contacts were formed by vacuum evaporation to fabricate SiO_2/GaN MOS capacitors. Although there was no damaged layer on the surface of the Ga-polar epilayer, we fabricated GaN MOS capacitors with and without the damage removal process to evaluate the effect of the process. Capacitance–voltage (C–V) and current–voltage (I–V) characteristics were measured at room temperature to investigate the electrical properties of the fabricated MOS capacitors. In addition, the energy band alignment of the SiO_2/GaN structures was studied by SR-XPS. For this purpose, the SiO_2 layers subjected to PDA were thinned to about 2 nm by dipping the samples in a diluted HF solution because XPS is a surface-sensitive technique. SR-XPS analysis was performed at BL23SU in SPring-8.[30] The radiation energy was 1253.6 eV, and the

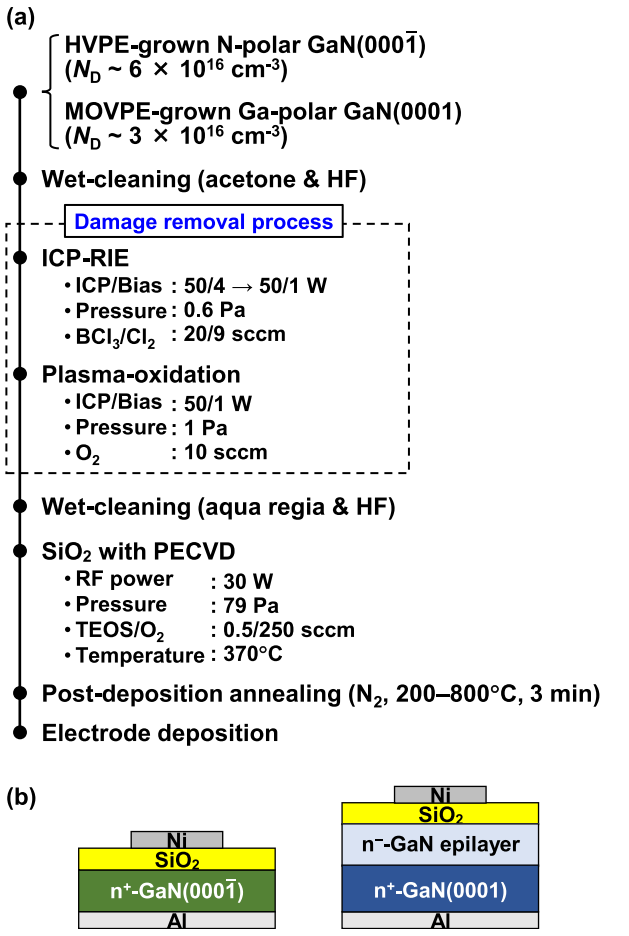

FIG. 1. (a) Fabrication process flow of GaN MOS capacitors on N-polar (000$\bar{1}$) and Ga-polar (0001) substrates. (b) Schematic illustrations of the fabricated N-polar GaN (000$\bar{1}$) and Ga-polar GaN (0001) MOS structures.

takeoff angle was set to 90°. The binding energy of the acquired spectra was calibrated with the peak energy (397.5 eV) of the N 1s core-level spectra corresponding to the Ga-N binding component of the GaN substrate.

Figures 2(a) and 2(b) show the bidirectional C–V curves of the SiO_2/GaN MOS capacitors fabricated on the GaN(000$\bar{1}$) and (0001) substrates, respectively. The measurement frequency was 1 MHz. Note that both N- and Ga-polar surfaces were subjected to the damage removal process shown in Fig. 1. For the reference SiO_2/GaN(0001) MOS capacitors in Fig. 2(b), the as-deposited sample exhibited small C–V hysteresis, which completely disappeared after PDA treatment at 800 °C. The C–V curves were mostly identical to those obtained from the epilayer without the damage removal process (data not shown) and consistent with our previous experiments.[29,31] These results demonstrate the feasibility of the damage removal process for preparing initial GaN surfaces for MOS device fabrication. Meanwhile, for the SiO_2/GaN(000$\bar{1}$) MOS capacitors, the C–V curve of the as-deposited sample showed apparent C–V hysteresis and a small hump in the forward sweep [see black lines in Fig. 2(a)]. Such hysteresis and humps

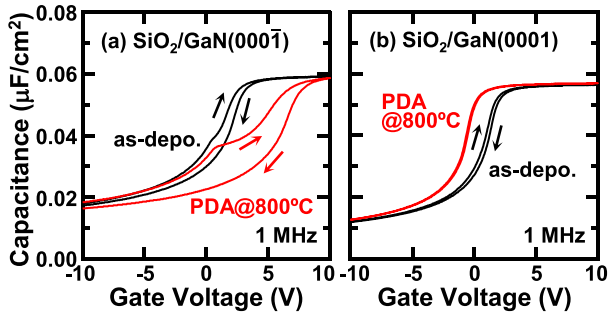

FIG. 2. Bidirectional C–V curves of SiO_2/GaN MOS capacitors fabricated on (a) N-polar (000$\bar{1}$) and (b) Ga-polar (0001) substrates. The measurement frequency was 1 MHz. Samples as-deposited and treated with PDA at 800 °C are represented by black and red curves, respectively.

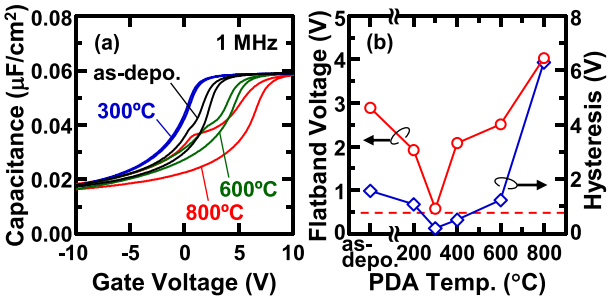

FIG. 3. (a) Typical C–V characteristics of SiO_2/GaN(000$\bar{1}$) MOS capacitors subjected to PDA at 300–800 °C. (b) PDA temperature dependence of V_{FB} and C–V hysteresis. V_{FB} was evaluated from $1/C^2$–V plots, and C–V hysteresis was calculated by taking the difference between the V_{FB} values for the forward and backward sweeps. The horizontal dashed line indicates the ideal V_{FB} position.

were found in all of the as-deposited SiO_2/GaN(000$\bar{1}$) MOS capacitors (data not shown). In addition, the PDA treatment at 800 °C significantly deteriorated the SiO_2/GaN interface, leading to severe C–V hysteresis, a stretched-out shape, and a prominent hump as indicated by the red lines in Fig. 2(a). We evaluated the C–V characteristics of a considerable number of MOS capacitors and obtained the similar results to those shown in Fig. 2(a). Thus, this fact has confirmed that the humps and large hysteresis in the C–V curves of SiO_2/GaN(000$\bar{1}$) MOS capacitors are not accidental characteristics caused by local defects in the GaN substrates but their intrinsic electrical properties. Comparison with the ideal C–V curves shows that electron trapping resulting in the humps occurred when the surface potential of GaN was bent upward by about 0.5 eV. Moreover, the electron trap densities were evaluated from the hysteresis of the C–V curves in Fig. 2(a) to be about 5×10^{11} and $2 \times 10^{12}\,cm^{-2}$ in the as-deposited and annealed N-polar GaN samples, respectively. These findings indicate that the SiO_2/GaN(000$\bar{1}$) structures are thermally unstable, even though the GaN(000$\bar{1}$) surface itself has high thermal stability. As previously reported, an ultrathin gallium oxide (GaO_x) interlayer forms at the SiO_2/GaN interface in the initial stage of SiO_2 deposition by PECVD.[29,32] Therefore, the difference in the electrical properties of the SiO_2/GaN(000$\bar{1}$) and (0001) MOS capacitors suggests that the formation process and/or thermal stability of the ultrathin GaO_x interlayer are dependent on the polarity of GaN surfaces. Actually, theoretical and experimental studies have already shown that the oxygen adsorption on the GaN surface differs depending on the polar surface.[33,34] To clarify the physical origin of interface defects resulting in the hump and hysteresis of the C–V curves, it is essential to compare theoretical calculations with the experimental results. However, the study on the origins of the interface states and defects observed in the C–V characteristics is beyond the scope of this Letter, and hence, we would like to discuss it elsewhere.

To explore optimal annealing conditions for GaN MOS devices on an N-polar (000$\bar{1}$) substrate, we examined the dependence of the PDA temperature on the electrical characteristics. Figure 3(a) shows the bidirectional C–V curves of the SiO_2/GaN(000$\bar{1}$) MOS capacitors subjected to PDA at temperatures ranging from 300 to 800 °C. While moderate C–V hysteresis was observed in the as-deposited sample as mentioned above, the hysteresis greatly improved after the PDA treatment at 300 °C, in which the C–V curve slightly shifted in the negative bias direction (see a blue curve). The PDA treatment at higher temperatures resulted in a large positive shift of the C–V curves and a significant increase in the C–V hysteresis. The flatband voltage (V_{FB}) of the C–V curves was determined from the $1/C^2$ vs gate voltage ($1/C^2$–V) plots, and the C–V hysteresis was also evaluated from the difference between the V_{FB} values determined from the forward and backward sweeps. Figure 3(b) shows the PDA-temperature dependence of the obtained V_{FB} and C–V hysteresis. In the figure, the ideal V_{FB} value (~0.5 V) for Ni/SiO_2/GaN(000$\bar{1}$) MOS capacitors is represented by the horizontal dashed line. The V_{FB} of the as-deposited sample shifted in the positive direction relative to the ideal value. As the PDA temperature increased up to 300 °C, the V_{FB} values gradually shifted in the negative bias direction and was almost equal to the ideal value after the PDA treatment at 300 °C. However, the positive shift in V_{FB} was observed again when the PDA treatment was performed at temperatures higher than 300 °C. The C–V hysteresis showed a similar tendency to V_{FB}, decreasing from as-depo. to 300 °C and increasing from 300 to 800 °C. The deviation from the ideal V_{FB} value and the magnitude of the C–V hysteresis are related to the fixed charge density and the trap density near the oxide/semiconductor interface, respectively.[35] Therefore, the optimal PDA temperature for GaN MOS structures on N-polar (000$\bar{1}$) substrates should be around 300 °C in terms of interface electrical properties, which is much lower than that for Ga-polar (0001) substrates (around 800 °C). Note that the PDA at a lower temperature of 300 °C than the SiO_2 deposition temperature of 370 °C improved the electrical properties of SiO_2/GaN(000$\bar{1}$) structures. This could be explained by the fact that the SiO_2 deposition was performed in a radical oxygen atmosphere for about 1 min, during which the growth of the unstable GaO_x interlayer on a GaN(000$\bar{1}$) substrate was caused, whereas the PDA was carried out in the nitrogen ambient for 3 min, which did not induce the GaO_x interlayer growth, leading to the superior C–V characteristics simply by thermal recovery of electrical defects near the interface and in the deposited SiO_2 dielectric. Meanwhile, degradation caused by the PDA treatment above 300 °C can be attributed to instability of the GaO_x interlayer formed on the GaN(000$\bar{1}$) surface, unlike that on the GaN(0001) surface, and/or subsequent Ga diffusion into the SiO_2 layer to form electrical defects in the gate oxide.[36]

Next, we compared the C–V characteristics of SiO_2/GaN(000$\bar{1}$) and (0001) MOS capacitors subjected to PDA at each optimized

temperature. Figures 4(a) and 4(b) show the frequency dispersion of the C–V characteristics of the GaN MOS capacitors fabricated on the (000$\bar{1}$) substrate with PDA at 300 °C and on the (0001) substrate with PDA at 800 °C, respectively. C–V characteristics were obtained at measurement frequencies ranging from 10 kHz to 1 MHz. The frequency dispersion of the SiO_2/GaN(000$\bar{1}$) MOS capacitor was negligible, similar to that of the SiO_2/GaN(0001) MOS capacitor. The interface state density (D_{it}) evaluated using the conductance method was below the detection limit of our measurement system ($D_{it} < 10^{11}\,cm^{-2}eV^{-1}$) for both fabricated MOS capacitors (data not shown). Figure 4(c) also shows the relationship between leakage current density (J) and oxide electric field (E_{ox}) for the GaN MOS capacitors fabricated on the (000$\bar{1}$) and (0001) substrates with the optimal PDA conditions. E_{ox} was calculated from $E_{ox} = (V_G - V_{FB})/CET$, where V_G is the applied gate voltage and CET is the capacitance equivalent thickness. Although the MOS capacitor on the (000$\bar{1}$) substrate showed a small leakage current even under the low electric field, which was defect-related, the leakage current was less than 10^{-7} A/cm^2 up to 6 MV/cm, indicating sufficient insulating properties for both MOS capacitors. The breakdown field was about 8 MV/cm for both cases. Note that both MOS capacitors showed a rapid increase in leakage current under the high electric field as a result of Fowler–Nordheim (FN) tunneling. The FN tunneling current (J_{FN}) is given by the following equation:[37]

$$J_{FN} = \frac{q^3 E_{ox}^2 m_0}{8\pi h \Phi_B m_{ox}} \exp\left(-\frac{8\pi\sqrt{2m_{ox}\Phi_B^3}}{3qhE_{ox}}\right), \quad (1)$$

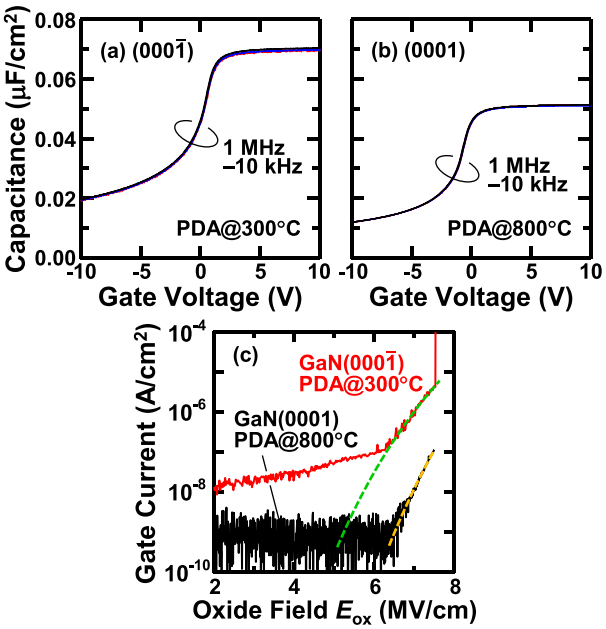

FIG. 4. Bidirectional C–V curves taken from SiO_2/GaN MOS capacitors fabricated on (a) GaN(000$\bar{1}$) and (b) GaN(0001). The GaN(000$\bar{1}$) and (0001) samples were subjected to PDA at 300 and 800 °C, respectively, for 3 min in N_2 ambient. Multifrequency measurements ranging from 10 kHz to 1 MHz were carried out. (c) J–E_{ox} characteristics of capacitors shown in figures (a) and (b). The dotted lines indicate the component of J_{FN} represented by Eq. (1) in the text.

where h is Planck's constant, q is the elementary charge, m_{ox} is the effective electron mass in the oxide layer, and Φ_B is the barrier height. m_{ox} of 0.42 × m_0 was used,[38] where m_0 is the free electron mass. Equation (1) means that Φ_B can be determined from the slope of the linear regression by plotting $\ln(J_{FN}/E_{ox}^2)$ against $1/E_{ox}$ (called the FN plot) and fitting the plot in the high E_{ox} (or low $1/E_{ox}$) region with the regression line. Therefore, we evaluated Φ_B from the J–E curves of samples fabricated under the optimal conditions determined from the results of the C–V measurements. Moreover, the J_{FN} was also calculated with Eq. (1) using Φ_B obtained from the FN plot. In Fig. 4(c), the calculated J_{FN} is represented by the dashed lines. Since the experimental curves in the high E_{ox} region can be fitted well with the theoretical lines, the evaluation of Φ_B from the FN tunneling current would be sufficiently reliable. The obtained values of Φ_B are 2.11 eV for the SiO_2/GaN(000$\bar{1}$) and 2.91 eV for the SiO_2/GaN(0001), corresponding to the change in the conduction band offset (ΔE_c) at the SiO_2/GaN interface of 0.80 eV depending on the polarity of the GaN surfaces.

In the previous section, we suggested from the J–E characteristics that the SiO_2/GaN(000$\bar{1}$) and GaN(0001) structures have different conduction band offsets, which may be due to the different behavior of the interface dipoles resulting from the opposite polarization of GaN substrates. Therefore, the energy band structures of SiO_2/GaN were evaluated from valence band spectra and O 1s energy loss spectra by SR-XPS measurement.[39] The valence band spectra obtained from the pristine GaN(000$\bar{1}$) and (0001) surfaces are shown as black lines in Figs. 5(a) and 5(b), respectively. Those of the SiO_2 layers (blue lines) were determined by subtracting the substrate spectra from the thin-SiO_2/GaN spectra (red lines). Then, the valence band offset (ΔE_v) was determined from the difference between the valence band maxima of GaN and SiO_2 as indicated in each figure. The obtained ΔE_v was 2.11 and 1.89 eV for the SiO_2/GaN(000$\bar{1}$) and (0001) structures, respectively. Figures 5(c) and 5(d) also show the O 1s energy loss spectra taken from the SiO_2 surfaces on GaN(000$\bar{1}$) and (0001) substrates, respectively. The deduced energy bandgap (E_g) of SiO_2 was 8.46 and 8.78 eV, respectively, for those on the (000$\bar{1}$) and (0001) substrates, which is likely due to the difference in the PDA temperatures optimized for the MOS structures on GaN(000$\bar{1}$) and (0001). More specifically, densification of as-deposited SiO_2 and that treated with PDA at 300 °C remained insufficient, but that treated with higher temperature PDA at 800 °C became dense and exhibited the ideal wide energy bandgap.[40,41] By taking the measured values and the reported E_g of GaN (3.39 eV) into account,[42] we can draw the energy band diagrams for SiO_2/GaN structures, as shown in Figs. 5(e) and 5(f). The obtained ΔE_c for the SiO_2/GaN(000$\bar{1}$) and (0001) structures was 2.96 and 3.50 eV, respectively. Although the absolute values of ΔE_c are different from those determined from the FN plots, ΔE_c of the SiO_2/GaN(000$\bar{1}$) structure is about 0.5 eV smaller than that of the SiO_2/GaN(0001) structure. Note that, even when assuming an identical E_g for SiO_2 films on the GaN(000$\bar{1}$) and (0001) substrates, ΔE_c of the SiO_2/GaN(000$\bar{1}$) is smaller than that of the SiO_2/GaN(0001). This means that, at high electric field above 6 MV/cm, gate leakage current larger than that of MOS devices fabricated on a GaN(0001) substrate is an intrinsic problem for MOS devices fabricated on a GaN(000$\bar{1}$) substrate. It should be noted that, since the leakage current determines gate oxide reliability, GaN MOS devices fabricated on a GaN(000$\bar{1}$) substrate have serious drawbacks in terms of reliability and limitation on process temperature.

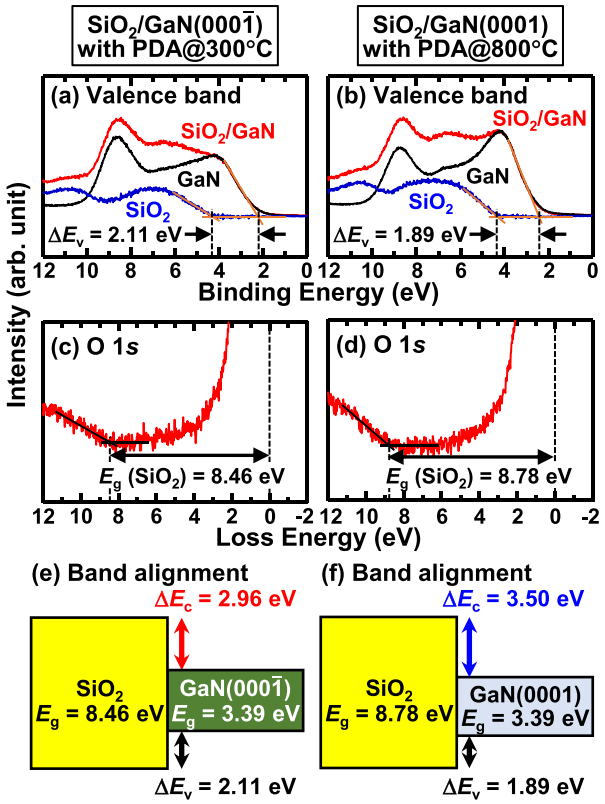

FIG. 5. (a) Valence band and (c) O 1*s* energy loss spectra taken from the SiO_2/GaN(000$\bar{1}$) structure, and (b) and (d) those taken from the SiO_2/GaN(0001) structure. Energy band diagrams of (e) SiO_2/GaN(000$\bar{1}$) and (f) SiO_2/GaN(0001) structures obtained by SR-XPS analysis.

In conclusion, we evaluated the electrical properties and energy band alignment of SiO_2/GaN(000$\bar{1}$) and (0001) MOS structures. The interface properties of GaN MOS structures differed greatly depending on the polar surface, and the SiO_2/GaN(000$\bar{1}$) structure was found to be thermally unstable. However, a very low D_{it} could be attained by optimizing PDA temperature. We also revealed that gate leakage current significantly increased for the SiO_2/GaN(000$\bar{1}$) MOS capacitors due to the reduction of the conduction band offset at the interface. Although GaN-based devices fabricated on a (000$\bar{1}$) surface are advantageous for high frequency operation and reducing the resistivity of Ohmic contacts, the application of GaN(000$\bar{1}$) to MOS power devices may present some challenges.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Hidetoshi Mizobata: Data curation (equal); Formal analysis (equal); Investigation (equal); Validation (equal); Visualization (lead); Writing – original draft (lead); Writing – review and editing (equal). **Kazuki Tomigahara:** Data curation (equal); Formal analysis (equal); Investigation (equal); Validation (equal); Visualization (supporting). **Mikito Nozaki:** Data curation (supporting); Formal analysis (supporting); Investigation (supporting). **Takuma Kobayashi:** Formal analysis (supporting); Investigation (supporting); Writing – review and editing (supporting). **Akitaka Yoshigoe:** Investigation (supporting); Resources (equal). **Takuji Hosoi:** Conceptualization (equal); Formal analysis (supporting); Investigation (supporting); Project administration (supporting); Writing – review and editing (supporting). **Takayoshi Shimura:** Formal analysis (supporting); Investigation (supporting). **Heiji Watanabe:** Conceptualization (equal); Formal analysis (supporting); Investigation (supporting); Project administration (lead); Supervision (equal); Writing – review and editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

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